

## **ABSTRACT OF THE DISCLOSURE**

One embodiment of the present invention provides a system having a nonvolatile memory comprising a p type semiconductor substrate, an oxide layer over the p type semiconductor substrate, a nitride layer over the oxide layer, an additional oxide layer over the nitride layer, a gate over the additional oxide layer, two N+ junctions in the p type semiconductor layer, a source and drain respectively formed in the two N+ junctions, a first bit and a second bit in the nonvolatile memory, and accordingly at least two states of operation (i.e., erase and program) therefor. That is, one bit in the nonvolatile memory can either be in an erase state or program state. For erasing a bit, electrons are injected at the gate of the nonvolatile memory. For programming a bit, electric holes are injected or electrons are reduced for that bit. The present invention also provides a method for sensing and reading at least one bit in a nonvolatile memory comprising applying a bias voltage to the memory, detecting a threshold voltage or read current, comparing the threshold voltage with a reference voltage or comparing the read current with a reference current, and identifying the at least one bit as erased or programmed.

FINNEGAN  
HENDERSON  
FARABOW  
GARRETT &  
DUNNER <sup>LLP</sup>

1300 I Street, NW  
Washington, DC 20005  
202.408.4000  
Fax 202.408.4400  
[www.finnegan.com](http://www.finnegan.com)